Full Wave Analysis of Electromagnetic Coupling in Realistic RF Multilayer PCB Layouts using Cascaded Parallel Plate Waveguide Model

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Abstract **Realistic multilayer Printed Circuit Boards (PCBs) used in RF applications have large amount of metalization and a number of vias to provide good shielding and connectivity between nets in different layers. Taking advantage of these physical properties and using the equivalence principle, the multilayer PCB is modeled as a cascade of parallel plate waveguides with half-space regions residing above and below the PCB. Instead of formulating the problem in terms of electric currents in the horizontal metal layers, it is formulated using equivalent magnetic currents in the non-metallic regions of layer interfaces. The equivalent magnetic currents at the dielectric interfaces are expressed in terms of the Rao-Wilton-Glisson (RWG) basis functions. The electric currents flowing on the vias inside dielectric layers are assumed constant in the vertical direction. These vertical electric currents radiate TEM modes in the parallel plate environment. Integral equations based on simple parallel plate and free-space Green's functions enforcing the boundary conditions are set up and solved using the Method of Moments. The equivalent magnetic currents in each layer interact with currents in the adjacent layers only, thereby resulting in a "*chained-block-banded*" matrix. Excitation is provided through ports defined at each pair of pads, or between a pad and nearby ground. These ports are located only on the top and the bottom layers of the PCB where the circuit components and IC pins are mounted. This formulation requires the computation of the MoM matrix only once per frequency for any number of ports. Further, the solution for only those unknown equivalent magnetic currents around the port regions is required to obtain the N-port impedance parameter characterization of the PCB. Consequently, a memory efficient block matrix solution process can be used to solve problems of large size for a given memory. Realistic PCB example is given to illustrate the validity of this approach.**

I. INTRODUCTION

Full wave methods based on layered media integral equation (MoM) formulations are popular in the microwave and antenna community [1] - [4] to analyze multilayer circuits. The Green's function for multilayered media is quite complicated and is an extensively researched topic [5]-[7]. Added to its analytical complexity, numerical evaluation of multilayered Green's function is time consuming as well. Various approaches such as pre-computation and interpolation [2], asymptotic extraction, discrete complex image method [5], and simulated image method have been proposed to speed up the computation of multilayer Green's functions. Commercial tools based on layered media Green's functions (e.g. Momentum[1], IE3D[2], Ensemble[3], etc.) make use of some these techniques. In spite of the advances in numerical electromagnetic modeling of multilayered structures, the presently available computer hardware restricts applications of these techniques or tools to only a small subset of real-world, full board electromagnetic coupling problems. The reasons are not difficult to understand. Today's multilayered PCBs tend to have more metalized regions at layer interfaces to effectively make use of board real estate, and have hundreds to thousands of vias to provide shielding and vertical connections between different layers and to reduce cross-talk. This is even more true in the case of PCBs for RF applications wherein arbitrarily shaped metalizations called area-fills are widely used to improve the EMI/EMC (Electromagnetic Interference / Compatibility) performance. Most of the methods based on multilayer Green's functions require discretization of the planar metalized area. In addition, the vias have to be approximated as polygonal cylinders in these approaches. Hence, each cylindrical via will require a minimum of four unknowns (assuming a square cross-section) to model the vertical current and additional unknowns are required to model via to planar metal junctions. Since the above approaches result in a dense matrix equation to be solved, any increase in the number of unknowns limits their applications due to both storage and solution time constraints. In this work, we propose a

[1] Momentum™, HP EEsof, Santa Rosa, CA.
[2] IE3D™, Zeland Software, Fremont, CA.
[3] Ensemble™, Ansoft Corporation, Pittsburg, PA.

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simple model for a multilayer PCB as a cascaded parallel plate waveguide structure with cylindrical vias in each of the dielectric layers. Using the equivalence principle, in our approach, only the non-metallic regions of the layer interfaces need to be discretized and there is no need to model junctions involving planar and vertical electric currents.

II. FORMULATION

In this section, we first formulate the multilayer PCB problem in terms of an equivalent problem, followed by the Method of Moments procedure. Next we briefly discuss the excitation mechanism and the extraction of Z and S parameters of the PCB layout structure.

A. Equivalent problem

Consider a structure with five metal layers (though the formulation is quite general, valid for any number of layers, we restrict to five layers to illustrate the equivalent problem graphically) as shown in Fig. 1. All layers are assumed infinite in extent. The finiteness of the board can be modeled by having a moat of equivalent magnetic current around the periphery of the board. However, in most cases this assumption can be justified because of the presence of a number of shielding vias around the periphery of typical PCBs that help prevent radiation through lateral walls of the PCB. Each of the dielectric layers can have different heights and material properties. The metal is assumed to be perfect electric conductor (PEC) and the planar metalization thickness is assumed to be zero.

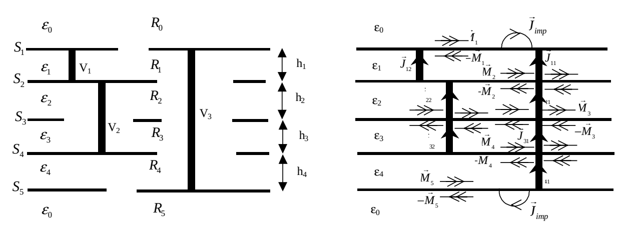

Figure 1 General multilayer PCB structure with vias: Original and Equivalent Problems

To apply the equivalence principle, the non-metallic regions (or the apertures) in each of the planar layer interface are short-circuited by PEC planes. Then the electric field in each aperture region is represented by equivalent magnetic current densities flowing on both sides of the PEC planes with the same magnitude but with opposite phase. Thus, in the equivalent problem, the multilayer structure becomes a cascade of parallel plate waveguide regions with half space regions at the top and bottom as shown in Fig. 1.

The equivalent magnetic currents and the vertical electric currents radiate in parallel plate waveguide regions (except $\mathbf{M_1}$ and $-\mathbf{M_5}$, which radiate in half-space regions). In a realistic board, the components and IC chips are mounted on the top and the bottom layers and hence the excitation is assumed to be present only on the top and/or the bottom layers. The equivalent magnetic currents at the layer interfaces and the electric current in the vias are the unknowns in the problem. By enforcing the continuity of tangential magnetic field at the interfaces and the total tangential electric field over the via surfaces in each of the parallel plate waveguide regions to be zero a set of coupled integral equations can be obtained. These coupled equations can be solved using the Method of Moments[9] procedure.

B. MoM Procedure

The equivalent magnetic currents residing at the layer interfaces are expanded over triangular elements using the RWG basis functions [8]. The electric current in each via within a dielectric layer is modeled as a single constant unknown vertical surface current, implying the fields radiated by the via will be dominant radial waveguide (TEM mode) type. The dielectric layer thickness in typical multilayer PCB structures is so small in terms of operating wavelength that this assumption is well justified. The fields due to the magnetic current and the vertical electric currents in the vias can be obtained from the Mixed Potential Integral Equation (MPIE) formulation using potential Green's functions for parallel plate waveguide and free-space region.

The set of coupled integral equations obtained from enforcing the boundary conditions can be solved using the standard Galerkin procedure [9], which results in the MoM matrix equation in (1).

$$\begin{pmatrix} [Y_{11}] & [YZ_{11}] & [Y_{12}] & [0] & [0] & [0] & [0] & [0] & [0] \\ [ZY_{11}] & [Z_{11}] & [ZY_{12}] & [0] & [0] & [0] & [0] & [0] & [0] \\ [Y_{21}] & [YZ_{21}] & [Y_{22}] & [YZ_{22}] & [Y_{23}] & [0] & [0] & [0] & [0] \\ [0] & [0] & [ZY_{22}] & [Z_{22}] & [ZY_{23}] & [0] & [0] & [0] & [0] \\ [0] & [0] & [Y_{32}] & [YZ_{32}] & [Y_{33}] & [YZ_{33}] & [Y_{34}] & [0] & [0] \\ [0] & [0] & [0] & [0] & [ZY_{33}] & [Z_{33}] & [ZY_{34}] & [0] & [0] \\ [0] & [0] & [0] & [0] & [Y_{43}] & [YZ_{43}] & [Y_{44}] & [YZ_{44}] & [Y_{45}] \\ [0] & [0] & [0] & [0] & [0] & [0] & [ZY_{44}] & [Z_{44}] & [ZY_{45}] \\ [0] & [0] & [0] & [0] & [0] & [0] & [Y_{54}] & [YZ_{54}] & [Y_{55}] \end{pmatrix} \begin{pmatrix} [M_1] \\ [J_1] \\ [M_2] \\ [J_2] \\ [M_3] \\ [J_3] \\ [M_4] \\ [J_4] \\ [M_5] \end{pmatrix} = \begin{pmatrix} [I_T] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [I_B] \end{pmatrix} \quad (1)$$

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Because of the equivalent formulation that we have employed, the MoM matrix has a "**chained-block-banded**" structure. For PCBs with more metalization and a large number of vias, this formulation leads to a matrix with far fewer unknowns and a faster solution of the matrix equation.

C. Excitation and Parameter Extraction

Traveling wave type excitation is not practical in realistic PCB structures since extending the reference plane of excitation is not always possible. Hence, we propose two types of localized current excitation schemes: (i) current loop injection and (ii) strip current excitation. Metal regions called Pads are used on the top and the bottom layers of the PCB board to mount discrete lumped components and IC chips. We define a port between a pad and nearby ground or across each pair of pads. A response voltage (V_{ij}) at the i^{th} port due to the excitation of the j^{th} port can be defined as the line integral of the electrical field along the line (called the port line) joining the endpoints of the i^{th} port current (I_j). If the triangular meshing is preformed in such a way as to have non-boundary edge(s) lying along the port line, then the electric field along the edge(s) is same as the unknown equivalent magnetic current defined on that edge(s), with the appropriate sign. Hence, the impedance parameter Z_{ij} can be obtained as the ratio of the voltage V_{ij} to I_j, from which the scattering parameter with respect to a reference impedance R_o (usually 50 Ω) can be computed using transformation equation [10].

The fact that only the unknown magnetic currents around the port regions are needed for the final characterization in terms of Z or S parameters, in conjunction with the chained-block-banded matrix equation with sparse right hand side, allows implementation of an efficient solution in terms of memory storage. Thus, one does not need to store all of the matrix blocks simultaneously. It is also to be noted that the MoM matrix need not be recomputed nor re-solved for any change in port locations or additional ports.

III. NUMERICAL EXAMPLE

Both serial and parallel (for shared memory machines using OpenMP directives) Fortran90 codes (which we call M3) based on the above formulation have been written. We have developed a geometry capture scheme to read in the geometry data directly from Mentor Graphics[1] that is widely used in the industry to make PCB layouts. It is to be noted that our formulation allows vias to be handled easily not only from the simulation point of view but also from the meshing viewpoint, as there is no physical contact between the vias and the meshed region.

A. Realistic Test PCB Layout

A realistic test PCB structure with four metal layers is the real-world example that we simulate using our code. The stack-up and the layouts of the four layers are shown in Fig. 2. We chose two nets, running close to each other, which start at the pads of a chip, run down two layers, and come back up onto the top layer. Ports 1 and 2 are defined at the ends of the first net and ports 3 and 4 are defined at the ends of the second net. For measurement purposes, the center conductors of four identical coaxial cables feed the four ports, with SMA connectors at the other end to connect to a Network Analyzer. The four port S-parameters of this system are measured using an HP 8753 Network Analyzer, after a full two port SOLT (short, open, load and through) calibration. This particular PCB has a large hole, which we neglect by assuming it is filled with the same dielectric layer and covered with metal at the layer interface. The mesh of the non-metallic regions of the four layers is shown in Fig. 3. The total number of unknowns in this problem is 11356 and it took about 30 minutes per frequency to solve the problem using eight CPUs on an SGI Origin 2000 machine.

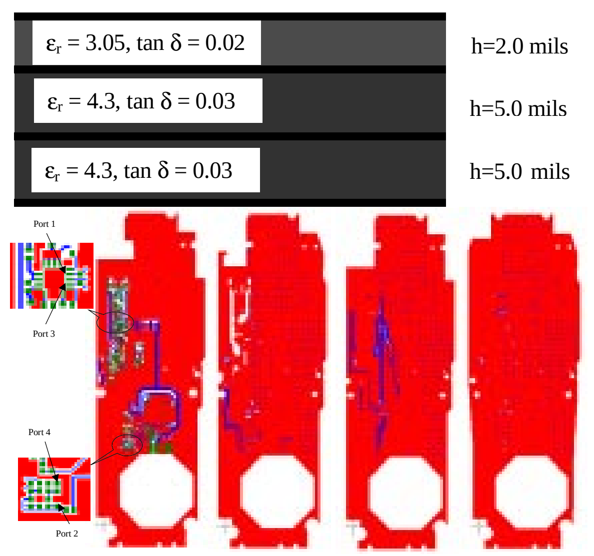

Figure 2 Stackup and Layout of realistic Test PCB

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[1] Board Station™, Mentor Graphics, Wilsonville, OR.

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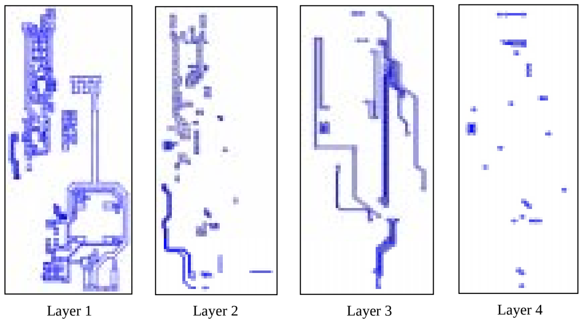

Figure 3 Mesh of non-metal region of the layers in the Test PCB

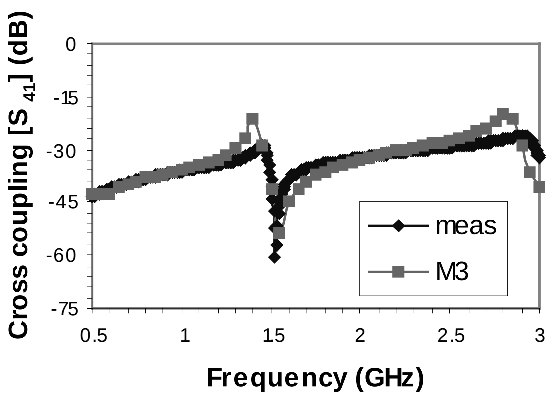

Figure 4 Cross coupling between ports 1 and 4 in the Test PCB

The cross-coupling between the ports 1 and 4 is shown in Fig. 4, which shows a good agreement between the prediction and the measurement. Through coupling and return loss predictions (not shown here) are found to have a qualitative agreement with the corresponding measured results. More examples and details of the formulation can be found in [11].

IV. CONCLUSIONS

In a real-world PCB, the presence of shielding and shorting vias, in addition to the signal vias, prevents radiation through the lateral walls. This gives us the freedom to assume anything outside the periphery of the board and we have assumed the infinitely long parallel plate waveguide model. Using these properties, we have presented a simple formulation to model electromagnetic coupling in a full PCB with a large number of vias and dense metalization very efficiently. The absence of direct physical contact between vias and the meshed non-metal region simplifies the meshing process as well. The storage efficiency of our method will increase with the number of layers, in contrast to the traditional dense MoM matrix formulation, where every unknown interacts with every other unknown directly.

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